



A Multi-DSP 96002 board

Herve Mathieu

► To cite this version:

Herve Mathieu. A Multi-DSP 96002 board. [Technical Report] RT-0153, INRIA. 1993, pp.59. inria-00070015

HAL Id: inria-00070015

<https://hal.inria.fr/inria-00070015>

Submitted on 19 May 2006

HAL is a multi-disciplinary open access archive for the deposit and dissemination of scientific research documents, whether they are published or not. The documents may come from teaching and research institutions in France or abroad, or from public or private research centers.

L'archive ouverte pluridisciplinaire **HAL**, est destinée au dépôt et à la diffusion de documents scientifiques de niveau recherche, publiés ou non, émanant des établissements d'enseignement et de recherche français ou étrangers, des laboratoires publics ou privés.



UNITÉ DE RECHERCHE
INRIA-SOPHIA ANTIPOLIS

Institut National
de Recherche
en Informatique
et en Automatique

2004 route des Lucioles
B.P. 93
06902 Sophia-Antipolis
France

Rapports Techniques

N°153

Programme 4

Robotique, Image et Vision

MD96 - A MULTI-DSP96002 BOARD

Hervé MATHIEU

mai 1993

MD96 - A Multi-DSP96002 BOARD

Hervé MATHIEU
INRIA-Projet Robotvis
bp 93
06902 Sophia Antipolis Cedex
Tel : 93 65 78 36 - Fax : 93 65 78 45
email hervem@sophia.inria.fr

May 10, 1993

Contents

1	MD96-TECHNICAL MANUAL	3
1.1	Introduction	3
1.2	MD96 Overview	3
1.3	DSP96002 Implementation	6
1.3.1	DSP96002 Overview	6
1.3.2	DSP96002 Mapping	6
1.4	Description of the MD96	7
1.4.1	Memory	7
1.4.2	Common Bus	7
1.4.3	DSP Host interface	8
1.4.4	Slave VMEbus Interface	8
1.4.5	Master VMEbus Interface	8
1.4.6	VMEbus Interrupt capability	9
1.4.7	DSP Interrupt facilities	9
1.4.8	Remote Reset	9
1.4.9	Use of the on-chip emulator : not yet implemented	9
1.5	Installation Guide of the MD96	9
1.5.1	Hardware necessities	9
1.5.2	On Board Jumper Installation	10
1.5.3	Note about Broadcast Capability	12
1.5.4	Software View	12
1.6	Some Figures about the MD96	13
1.6.1	Internal Access Time	13
1.6.2	VMEbus Access Time	13
1.6.3	Electrical and Mechanical Specification	15
1.6.4	Leds	15
1.6.5	MD96 Layout	16
1.7	System Integration and Communication	17
1.8	Future	17
2	MD96-SOFTWARE SUPPORT	19
2.1	Introduction	19
2.2	Software Installation	19
2.3	Building an application on the MD96	20
2.3.1	Host to MD96 code translation	20
2.3.2	MD96 mapping	21
2.3.3	How to Compile MD96 Code	22
2.3.4	Some C optimizations	24
2.4	MD96 On Board Library	25
2.4.1	VMEbus Access	25
2.4.2	Inter_DSP Communication	27
2.4.3	Communication between MD96 and Host	29
2.4.4	Inter_MD96 Communication	29
2.4.5	High Level Functions for MD96	30
2.5	MD96 Host Library	30
2.5.1	The Library	30
2.5.2	How to Compile on the Host machine with the MD96 library	34

2.6	Example of MD96 Applications	34
2.6.1	3x3 Convolution	34
2.6.2	Deriche Filter	35
2.6.3	Binocular Stereo Correlation	35
3	MD96-HARDWARE SUPPORT	37
3.1	Introduction	37
3.2	Hardware Description	37
3.2.1	Data Transfers	37
3.2.2	VMEbus Slave Interface	37
3.2.3	VMEbus Interruption	38
3.2.4	DSP Module	38
3.2.5	Internal mapping	39
3.2.6	VMEbus Mastering	39
3.2.7	Timing Philosophy	39
3.2.8	OnCE	40
3.2.9	Bugs or things which can be better	40
3.2.10	Hardware Bugs	40
3.3	Software Description	40
3.3.1	Detail of the address decoder logic	40
3.3.2	DSP Mapping View	41
3.3.3	VMEbus Mapping View	41
3.4	Reserved memory space description	47
3.4.1	For the X Data memory field	47
3.4.2	For the Y Data memory field	47
3.4.3	For the Common memory	48
3.5	Schematics, Layout and PLDs	49
3.5.1	Hierarchical Design	49
3.5.2	VMEbus Interface	50
3.5.3	DSP Module	53
3.5.4	OnCE Interface	54
3.5.5	Layout	55
3.5.6	Programmed Logic Device	56
3.5.7	Integrated Circuit	56

Chapter 1

MD96-TECHNICAL MANUAL

1.1 Introduction

MD96 is the name of the Multi-DSP 96002 board developed in Robotvis department (INRIA-Sophia), during ESPRIT P940 European project, in 1989.

The MD96 is a high integrated board, using four Motorola 96002 Digital Signal Processors and interfaced with the VMEbus.

This document is a general overview of the MD96, its synoptic, its performance and its installation guide, with also an overview of the processor used.

Two other chapters are about the MD96. A Hardware Annexes explains in details how the MD96 works, it includes the schematics and the PLDs equations. A Software support gives the C functions syntax of the MD96 library. These functions allows you to develop application on the MD96, it includes functions to connect the MD96 and the Host machine (SUN, VxWorks system, ...) and functions which are internal functions of the MD96 (inter DSP communication, VMEbus accesses, DMA transfer, ...).

This chapter consists of four parts :

- The first one provides a general view of the board. It explains the global architecture of the MD96, then a general view of the processor, and some information about its implementation are given.
- The second one gives a full description of the board, and explains the different element build around the data path on the MD96.
- The installation guide allows to insert the MD96 in a VMEbus system. Some figures about electrical consumption, mechanical, and data transfer timing specifications are also given.
- The fourth part gives generalities about System Integration, Communication, and about future expansion for the MD96.

The architecture of the MD96 allows a great reduction in terms of time computation in regard to a workstation, if they fit these requirements :

- Firstly, application must use the maximum of the DSP 96002 features. That means, to have a great amount of floating point operations, to use trigonometry (Look Up Table in the DSP 96002) or to accept perfectly DSP 96002 memory mapping (X,Y,P fields).
- Secondly, it must use the MD96 features. That means to be parallelized in a small number of tasks (between 4 and 16), to use the inter-DSP communication, not to be too greedy in terms of memory space (Only 9 Megabytes are available).

1.2 MD96 Overview

The MD96 is VMEbus interfaced board achieving a peak processing power of 240 MFLOPS.

The main features of the MD96 are :

- Four Processing Elements (PE), working in parallel. Each PE is composed of a 96002 Digital Signal Processor at 33 or 40 MHz and one or two JEDEC memory modules. The memory modules are organized in 64Kx32, 128Kx32 or 256Kx32. Thus, each DSP can have 2 Mbytes of fast static memory.
- A On Board Shared bus between the four PE, the VMEbus and a Common memory (64 Kwords to 256 Kwords). This Common memory is one JEDEC module of 64Kx32 up to 256Kx32. This Common bus allows PE to create fast communication channels between them and to share data using a Common memory. This memory could also be used by the VMEbus interface.
- Each PE can be master or slave on the VMEbus allowing the board to work without any master board. (except for boot operation). The VMEbus interface module is fully compliant with the VMEbus specification (Revision C.1). The interface is a module which is A32-D32 MASTER/SLAVE (allowing 32-bit data transfers), A24-D32 MASTER/SLAVE and A24-D16 MASTER.
- The Arbiter, Interrupter and Timer modules of the VMEbus specification are not provided on the DSP board.
- A Broadcast transfer can take place on the VMEbus to simultaneously access several MD96. It allows a simultaneous write into the Common memory. Because Broadcast transfer is not support by VMEbus, two external rows of the P2 connector are used to provide this feature.
- Remote Reset facility for each PE is provided.
- Interrupt generation facilities : The VMEbus interface is able to generate VMEbus interrupts with programming interrupt levels and vectors. This function is used by the PE to provide synchronism with the supervisor and is very efficient for real time application.
- Each PE module can be interrupted by VMEbus. In fact you can activate three different interruptions by DSP.
- A DSP OnCE (MOTOROLA Trademark) debug interface will be implemented on the MD96 to debug the DSPs. This interface is mapped into the VMEbus world register mapping able to access the serial OnCE DSP interface. This interface will be used later for high level debugging.
- There is no need for a bootstrap memory EPROM on the board, since each DSP will be start up from its Host interface. This feature saves four EPROM devices, but requires a Host intervention at RESET. It allows a complete reconfiguration of the board, both for the user program and the development tools.
- The MD96 is constituted of standard CMOS/TTL components only, and is implemented on a extended double Euro-Card (220 mm x 233 mm).

The MD96 accepts up to 9 Mega Bytes of fast access memory, which is useful to support C applications. It efficiently uses the dual port DSP capability. Each DSP can work in its Local memory (port B) with zero Wait State and no bus arbitration, and the Common bus (port A) can be used by each DSP with one Wait State, or by the VMEbus with a minimum of arbitration. (fig 1 summarize the MD96 hardware architecture).